Panel Discussion
- Multi-core strategy for the future -

Tera-scale Computing Research

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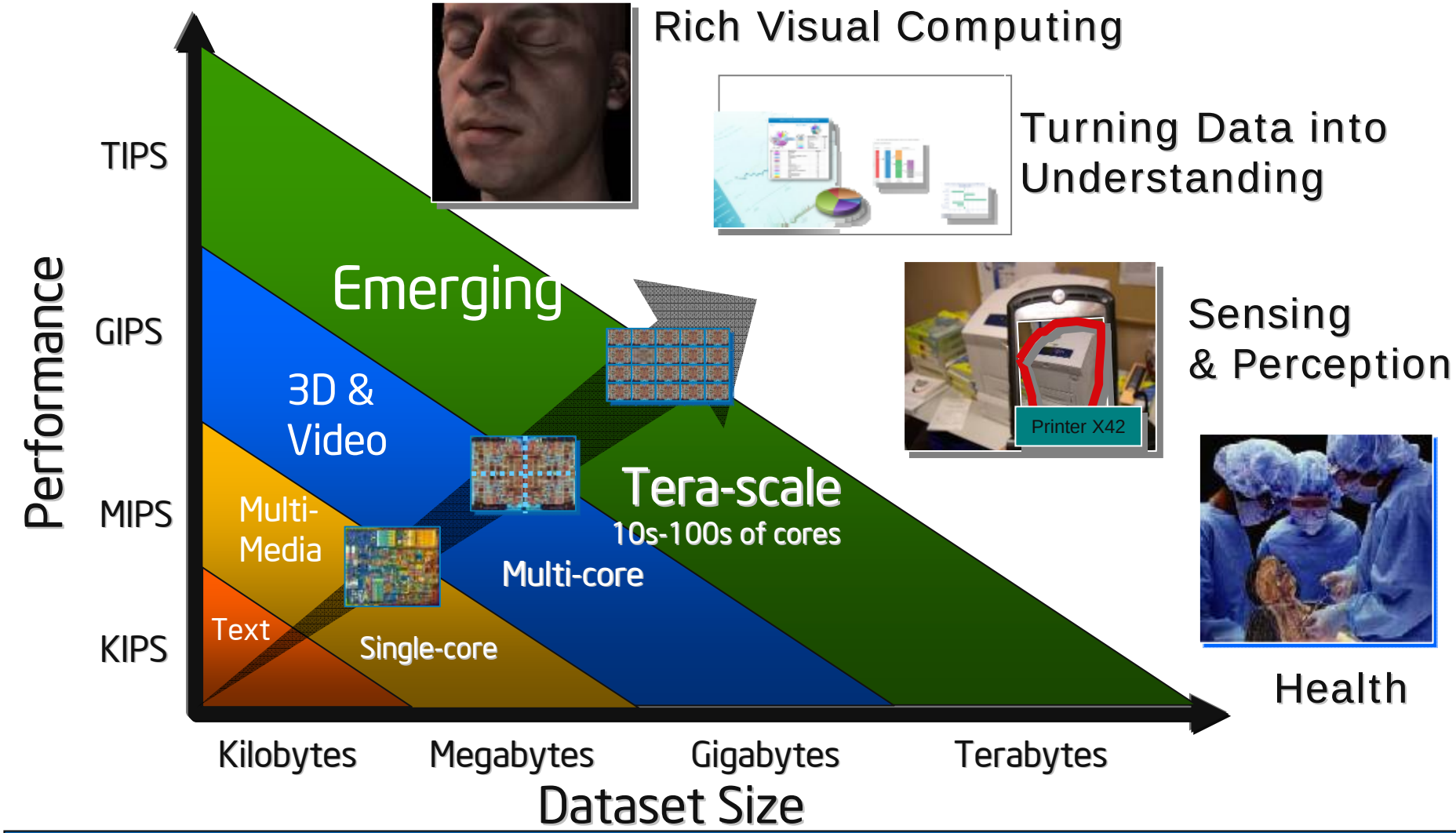
Agenda

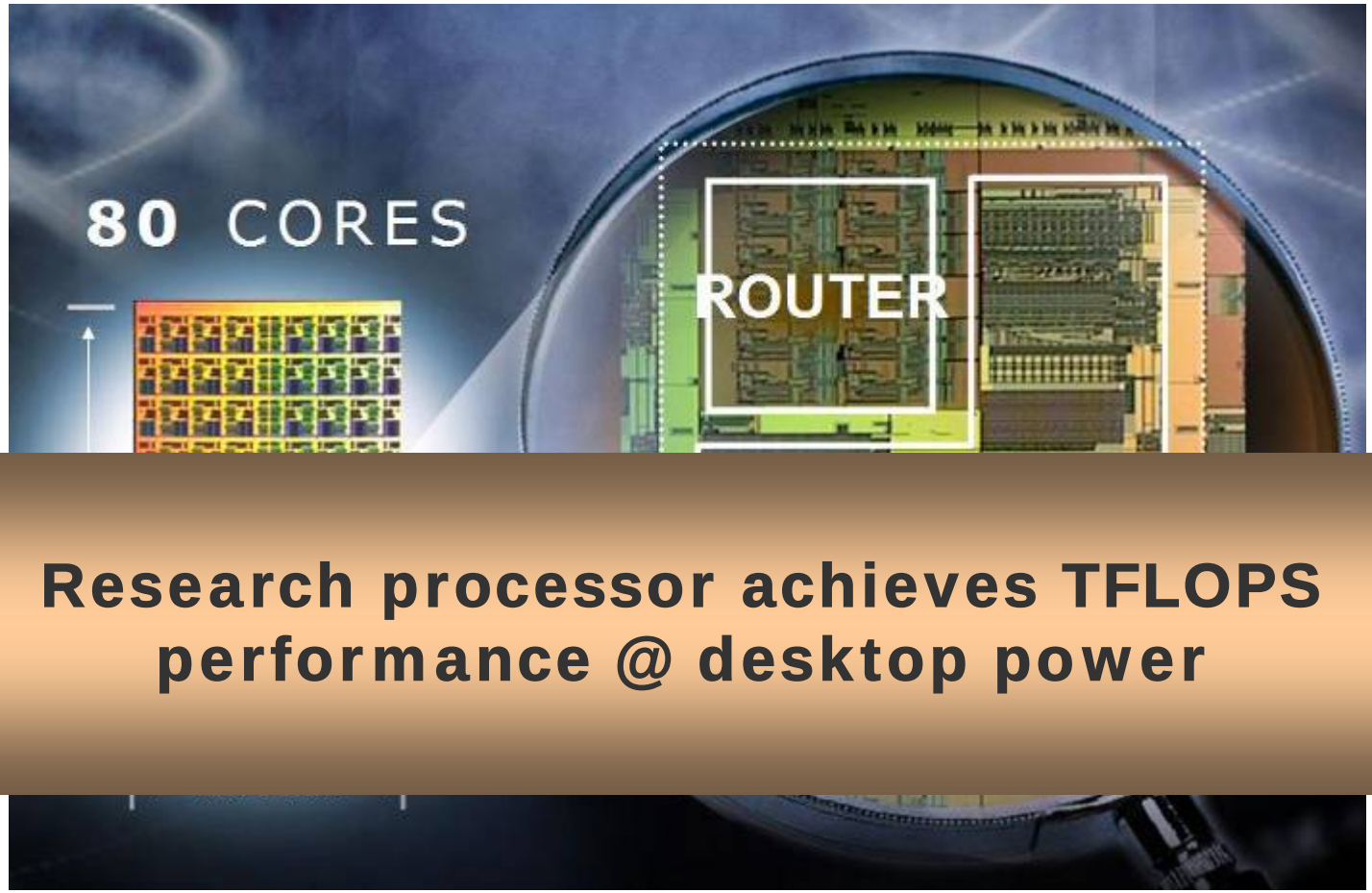
- Scope of Tera-scale computing research
- 80-core research chip
- Many efforts to enable many core
- Call to actions

Intel Tera-scale Research

Scaling multi-core to bring tera-scale performance the mainstream



TFLOPS demo at 62 Watts

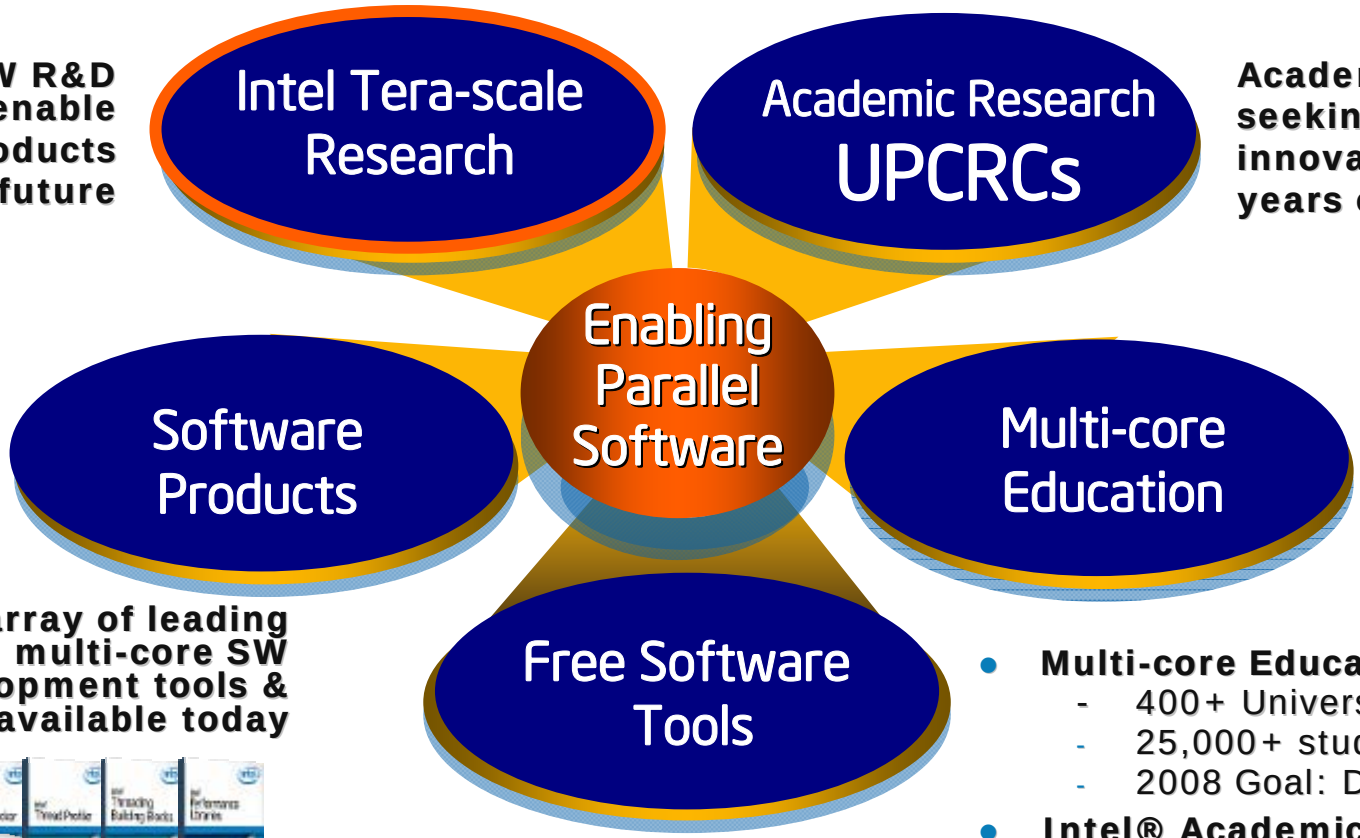


Research processor achieves TFLOPS performance @ desktop power

Essential step towards terascale multi-core processors!

Many efforts to enable many cores

Joint HW/SW R&D program to enable Intel products 3-7+ in future



Academic research seeking disruptive innovations 7-10+ years out

Wide array of leading multi-core SW development tools & info available today

- **TBB Open Sourced**
- **STM-Enabled Compiler on Whatif.intel.com**
- **Parallel Benchmarks at Princeton's PARSEC site**

- **Multi-core Education Program**
  - 400+ Universities
  - 25,000+ students
  - 2008 Goal: Double this
- **Intel® Academic Community**
- **Threading for Multi-core SW community**
- **Multi-core books**

Must work closely with customers, and industry and academic partners

Call to actions

- ***Hardware***
  - Memory bandwidth and I/O
    - Ex. 3D stack
  - High efficiency core to core communication
    - Ex. On die network
  - Power dissipation
    - Ex. Fine Grain Power Management / Core hoping
- ***Software***
  - Parallelism
  - Transactional Memory
  - Speculative multi-threading
- ***Joint Hardware & Software R&D***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