The Dataplane Processor Company

Customizable Dataplane Processors for System-on-Chip

テンシリカ株式会社
菅原 崇之

V10.3

Tensilica, Inc.

製品 – Customizable Processor IP

- Dataplane Processor Units (DPUs) IP cores: 低消費電力、小面積、ハイパフォーマンスなCPU/DSPコアとソフトウェアデザインツールを合わせて提供
- オーディオ、ビデオ、イメージング、ベースバンド向け、スタンダードDPUソリューション
- configurable processor technology について、40以上の特許

マーケット – Broad based success

- Consumer wireless, Home entertainment, Printing and digital imaging, Wireline network access, Networking infrastructure, Graphics GPUs and PC components

ビジネスモデル – 半導体IPライセンス

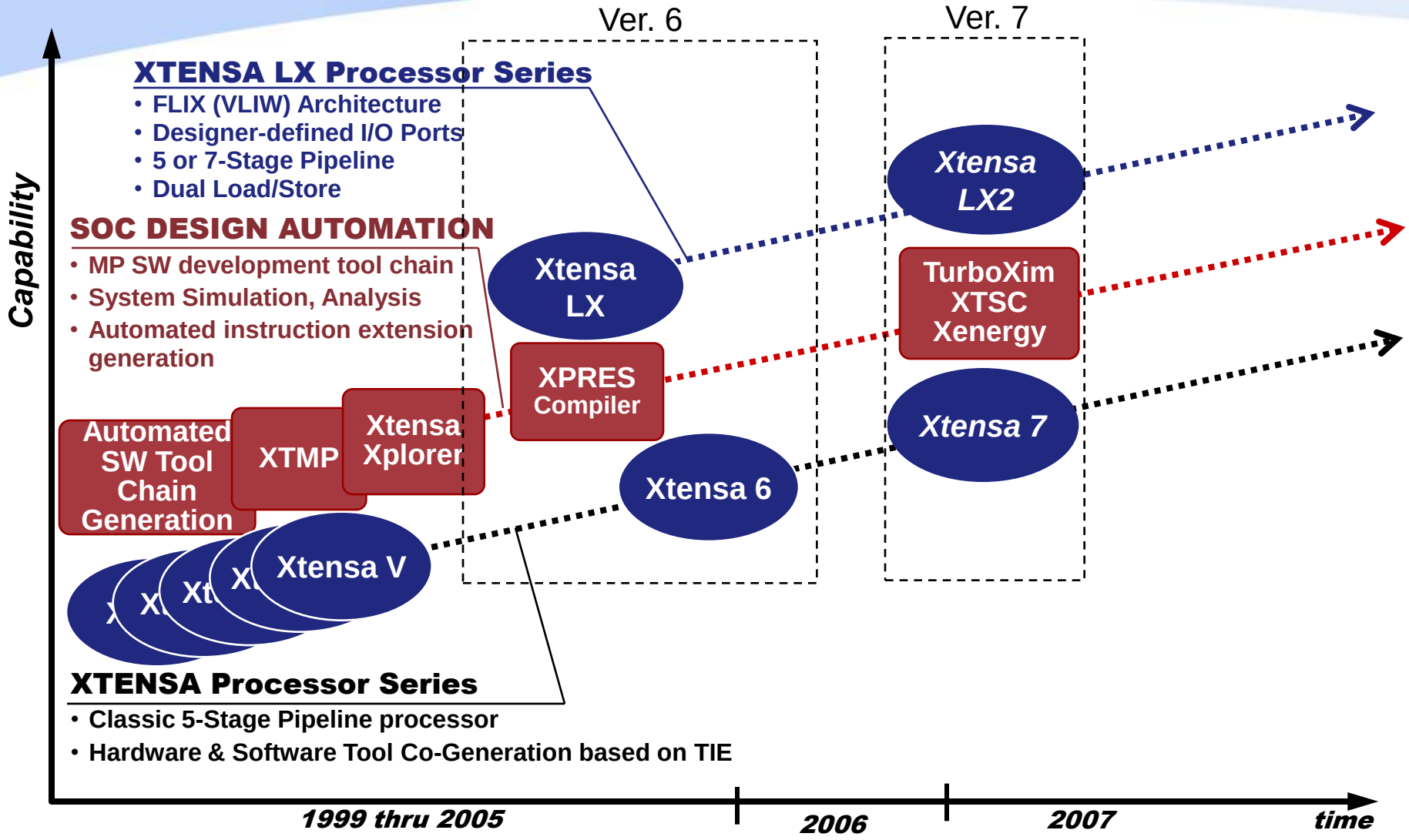
- 130社以上にライセンス(半導体トップ10企業の5社を含む)
- 年間2億個以上の出荷
- 最も成長率の高いプロセッサ/DSP IP企業 (2007年は22%成長)

会社概要

- 1997年設立、未上場
- 本社: カリフォルニア、サンタクララ
- 1999年日本法人設立(テンシリカ株式会社)

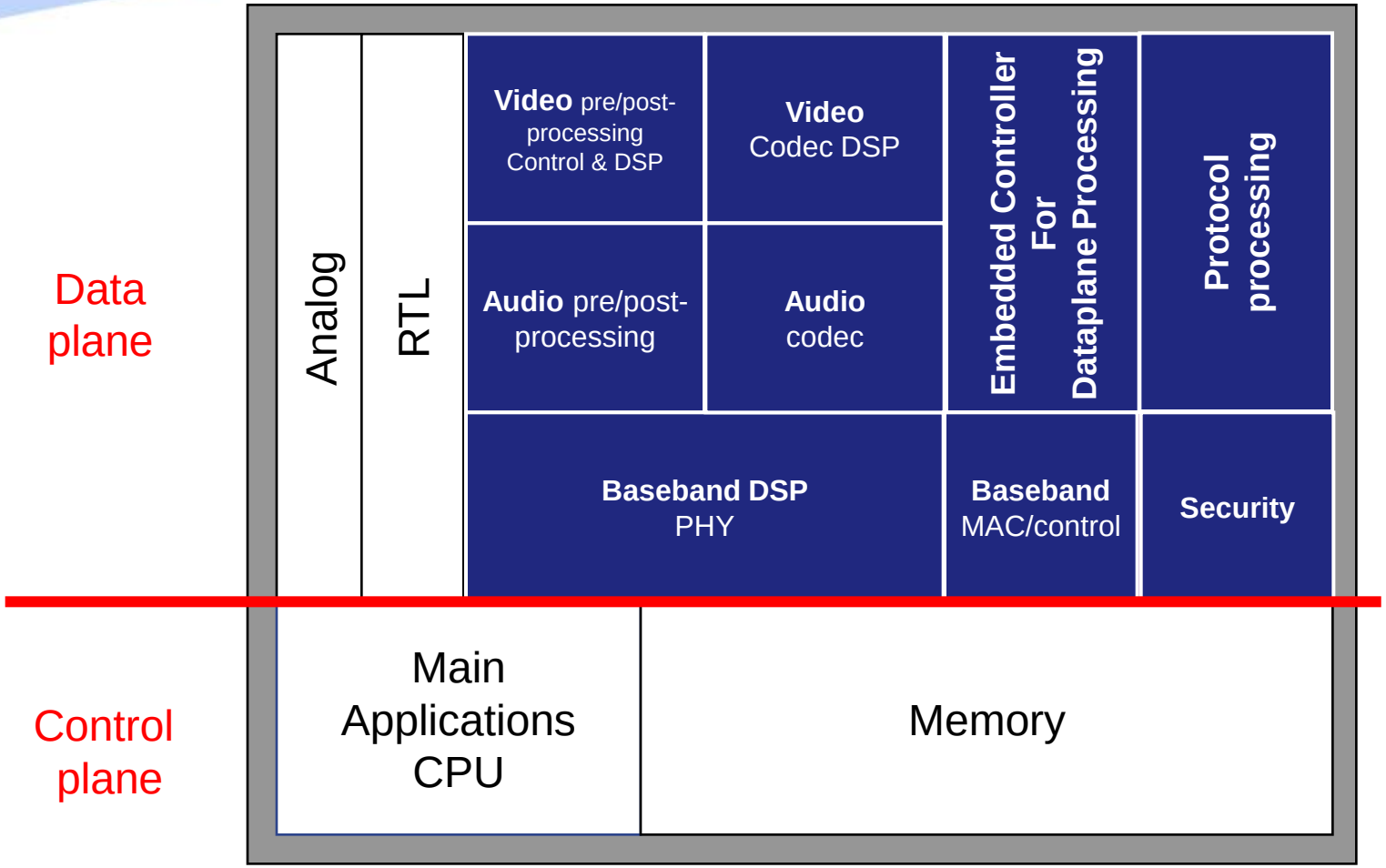
© 2008. Tensilica Inc.

Xtensa Processor Generator Evolution



© 2008. Tensilica Inc.

Tensilica Focus: Dataplane

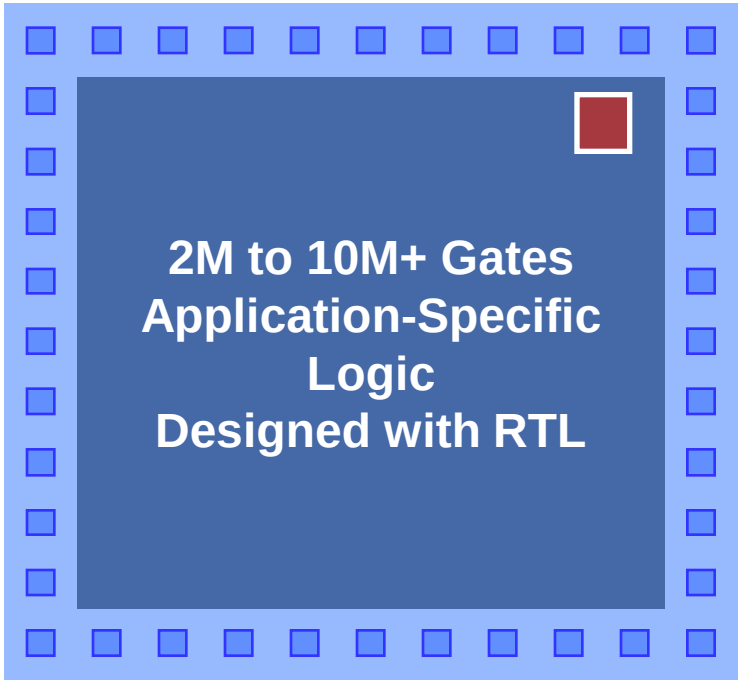


Tensilica fit and success – Embedded Control and DSP

© 2008. Tensilica Inc.

Complex SOCs: *Risk & Reward*

- ***Complex SOCs deliver many benefits***
  - High performance
  - Low cost and low power through integration
- ***Complex SOC design is risky***
  - Time to market – design productivity gap
  - Verification of millions of gates of custom logic



© 2008. Tensilica Inc.

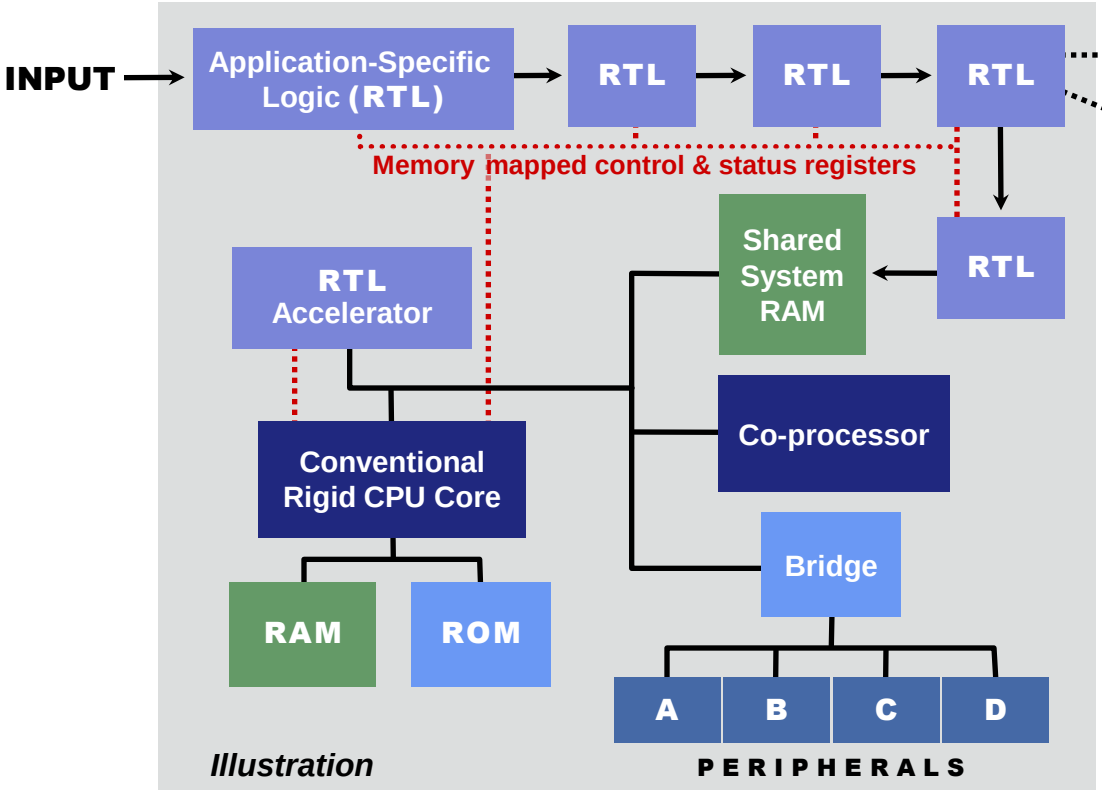
Fixed RTL Logic: *The Risk Factor*

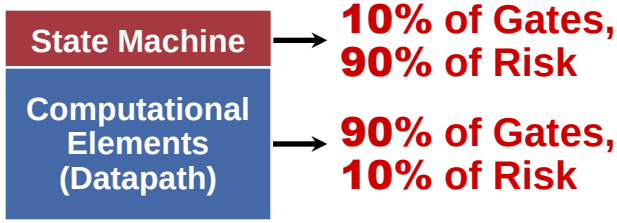
RTL Logic

…

… increases risk, slows time to market

- Verification of complex state machines
- Costly silicon respins to make changes
- Obsolescence as markets or standards change

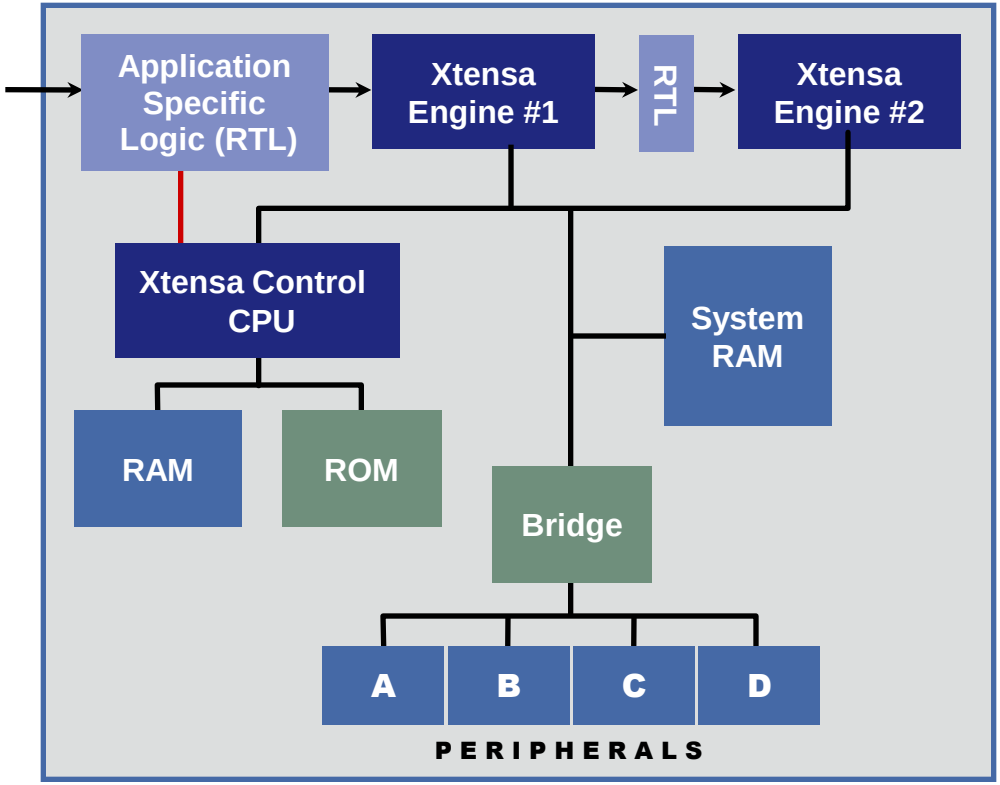




© 2008. Tensilica Inc.

Processor Solution for SOC Design

- ***Optimized Processors as Building Blocks***
  - Task-specific, optimized processors
  - Optimal performance/power/cost; similar to RTL performance
  - Hardware and Software Design productivity
- ***Lower Risk***
  - Verify Algorithm in Software within hours
  - Change in Software
- **Higher Productivity Design**



Bus topology shown for illustration purposes only
Numerous topologies and configurations possible

© 2008. Tensilica Inc.

Tensilica's Processor Technology

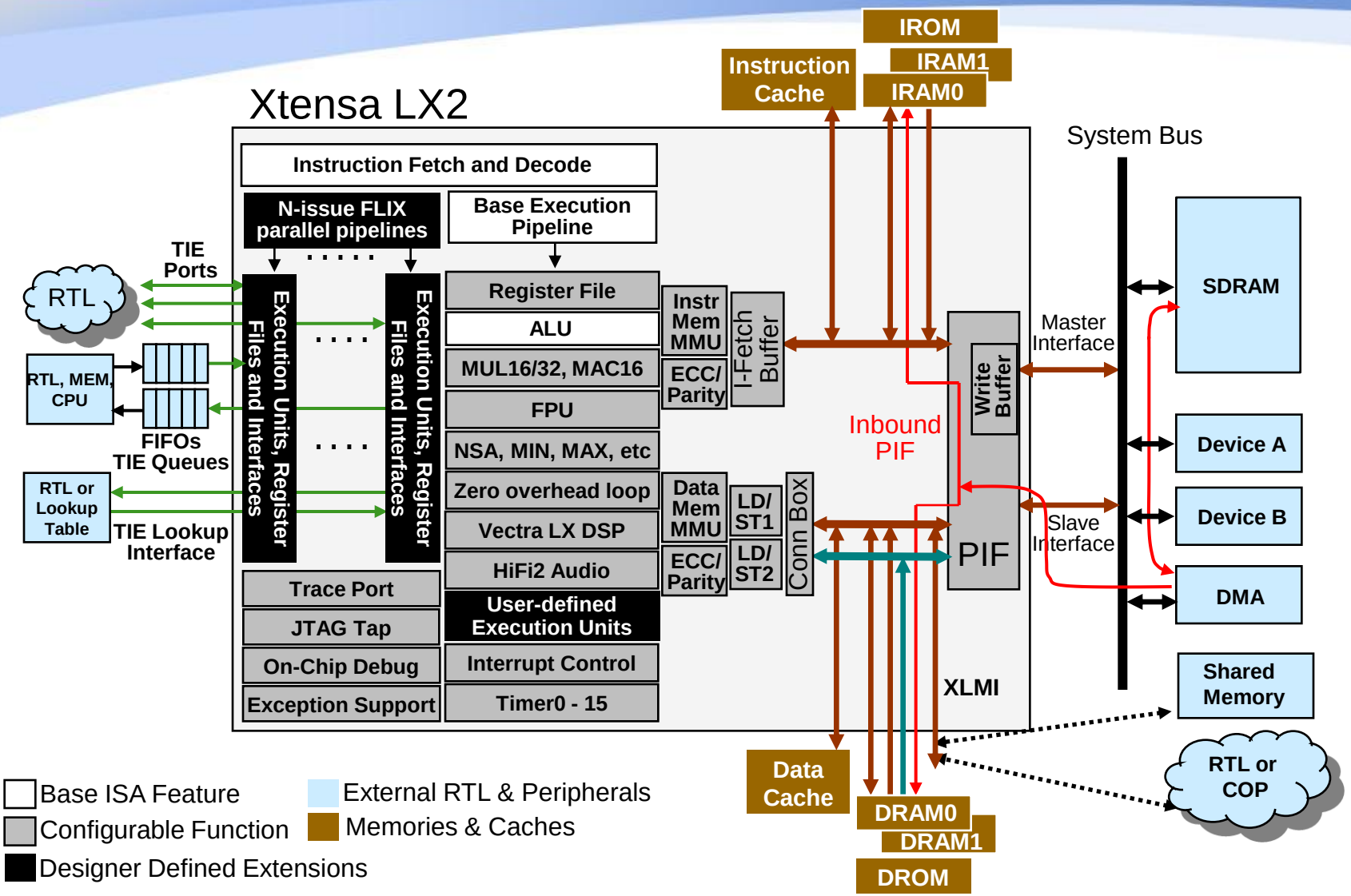
© 2008. Tensilica Inc.

Customizability

- **Configurability**
  - 予め用意された機能を選択
  - チェックボックス、ドロップダウンメニューで設定
- **Extensibility**
  - 実行ユニット、レジスタ、レジスタファイル、IOを追加し、命令の振る舞いを定義
  - TIE: Tensilica Instruction Extensionによる記述
- **CustomizabilityはConfigurabilityとExtensibilityの両方を含む概念**

© 2008. Tensilica Inc.

Xtensa LX2 Block Diagram:
Complete ISA and I/O Flexibility



© 2008. Tensilica Inc.

Xtensa Architecture: 3 Layer

- **Core ISA**
  - 32-bit RISC architecture
- **Configurable options**
  - Execution Unit and ISA options
  - Interface options
  - Memory Subsystem options
- **Processor extension**
  - Instruction
  - User Register, User Register File
  - I/O

© 2008. Tensilica Inc.

Xtensa Core ISA

- ハーバードアーキテクチャ
- 32ビットオペレーション
- 24ビット長命令
  - 16ビット長命令はオプション
- レジスタウインドウ
- 条件分岐命令
- 5段パイプライン
  - 7段パイプラインはオプション

© 2008. Tensilica Inc.

Xtensa Configurable Options

- レジスタファイル: 16/32/64エントリ
- ゼロオーバーヘッドループ
- MUL16/32, MAC16, DIV
- DSP engine, FPU
- PIF: Processor Interface, 32/64/128bit width
- I-Cache, D-Cache, Local Memory
- MMU
- Exception, Interrupt
- On-Chip Debug, Trace,
- …

© 2008. Tensilica Inc.

Processor Extension: TIE

- **TIE言語による拡張記述**
  - 命令の機能を記述
  - ユーザレジスタ
  - ユーザロードストア
  - ユーザIO(TIE port, TIE queue, TIE look-up)
    - ロードストアとは独立
  - パイプラインの追加 (3-issue VLIW)
- **機能レベルで記述**
  - Verilogライクにビット幅を明示
  - パイプラインステージを考慮する必要はない
  - TIE compilerがRTLを自動生成

© 2008. Tensilica Inc.

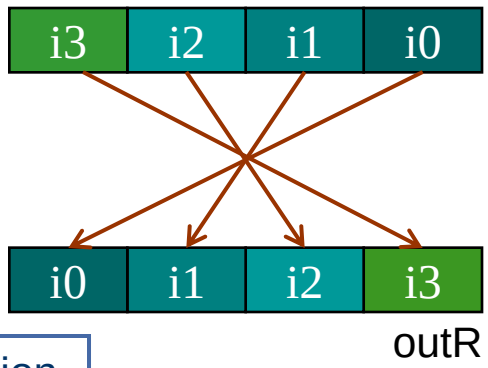
TIE

- ユーザ独自の命令をTIE言語を使うことにより拡張可能
- アプリケーションに特化した命令をもつことによる大幅な性能向上
- 作られた命令はユーザの独自ノウハウとなり、差別化が可能
- 親しみやすい記述仕様　Verilogのサブセット

＜TIE　記述例＞

```
operation BYTESWAP {out AR outR, in AR inpR}{}
{
  assign outR =

{inpR[7:0],inpR[15:8],inpR[23:16],inpR[31:24]};
```



The *operation* statement describes an entire new instruction, including:

1. Instruction name
2. Instruction format and arguments
3. Functional behavior [written in a Verilog subset]

© 2008. Tensilica Inc.

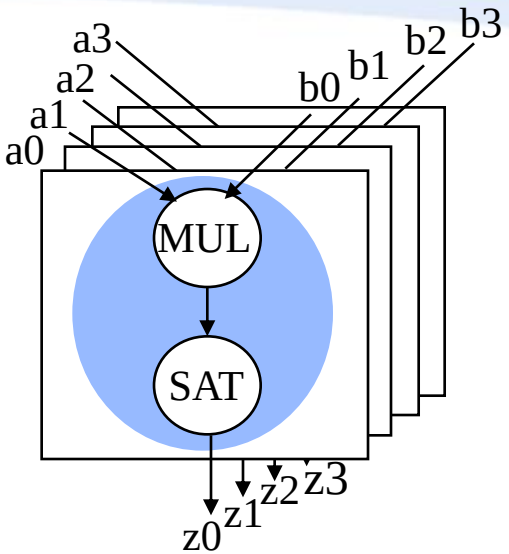
TIE: Wider SIMD Operations

User Defined 64bit Vector Register File

a	a3	a2	a1	a0
b	b3	b2	b1	b0
z	z3	z2	z1	z0

4-way SIMD 16x16 Mul-Saturate

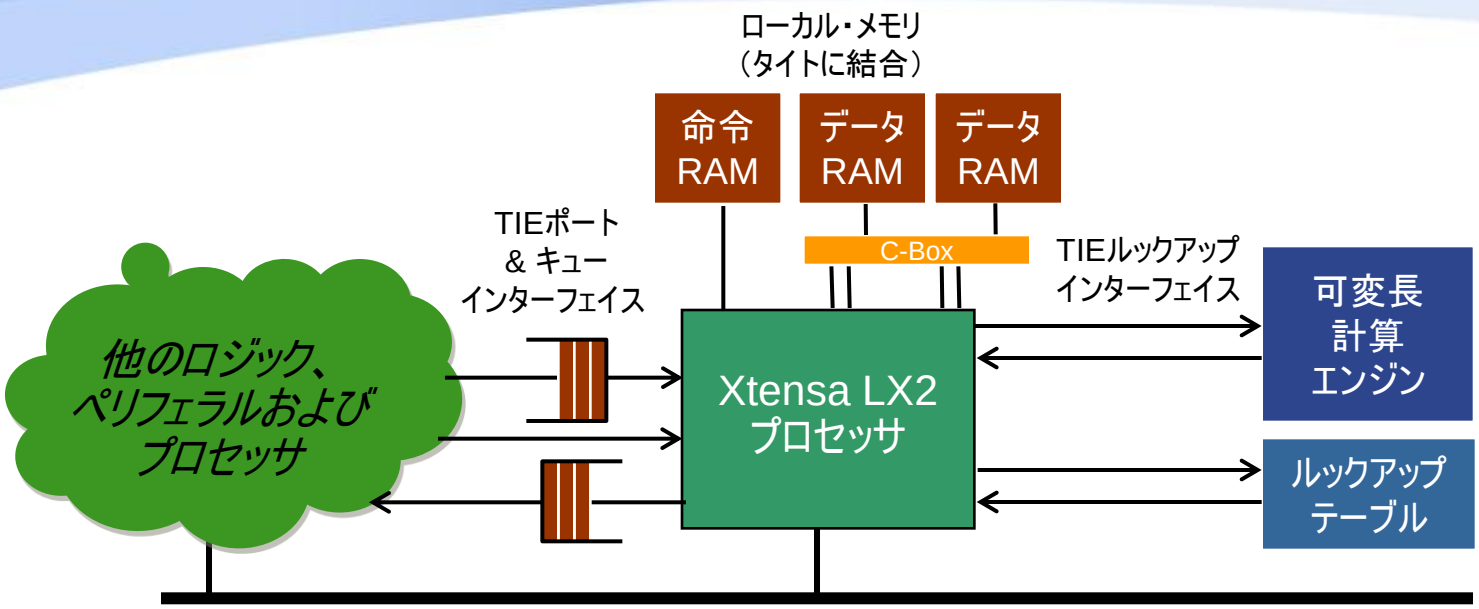
```
regfile VR 64 16 vr
operation MUL_SAT_4x16 {out VR z, in VR a, in VR b} {}
{
  wire [31:0] m3 = TIEmul(a[63:48],b[63:48],1);
  wire [31:0] m2 = TIEmul(a[47:32],b[47:32],1);
  wire [31:0] m1 = TIEmul(a[31:16],b[31:16],1);
  wire [31:0] m0 = TIEmul(a[15:0], b[15:0], 1);
  assign z =
    {m3[31] ? ((m3[31:23]==9'b1) ? m3[23:8] : 16'h8000)
            : ((m3[31:23]==9'b0) ? m3[23:8] : 16'h7fff),
     m2[31] ? ((m2[31:23]==9'b1) ? m2[23:8] : 16'h8000)
            : ((m2[31:23]==9'b0) ? m2[23:8] : 16'h7fff),
     m1[31] ? ((m1[31:23]==9'b1) ? m1[23:8] : 16'h8000)
            : ((m1[31:23]==9'b0) ? m1[23:8] : 16'h7fff),
     m0[31] ? ((m0[31:23]==9'b1) ? m0[23:8] : 16'h8000)
            : ((m0[31:23]==9'b0) ? m0[23:8] : 16'h7fff) };
}
schedule ms {MUL_SAT_4x16} {def z 2;}
```



- Create up to 24 register files, with 1024 registers each of width up to 1024 bits
- A new C data type is automatically created

© 2008. Tensilica Inc.

TIE: ユーザ定義I/O



従来のSOCバス（32-64b）

ルックアップ・ポート　新しいTIE 機能

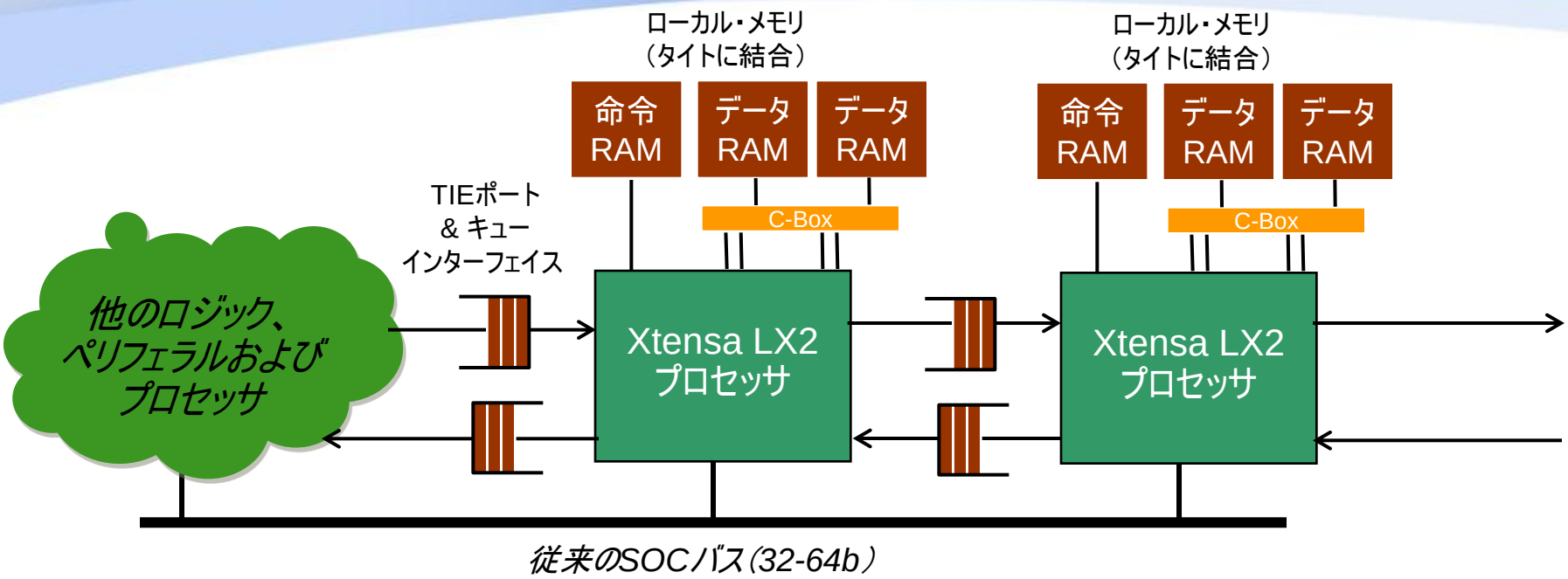
- 個別の命令/データ・メモリとは異なった、新しいメモリへのリード/ライト・インターフェイスを作成
- プロセッサ・データパスから直接、ロード/ストア命令とレイテンシを伴わずにリード/ライト

応用例

- メディアDSP – 係数テーブル、VLCエンジン
- ベースバンドDSP – プログラマブルなフィルタ係数
- ネットワーキング・アプリケーション– ルーティング・テーブル・ルックアップ

© 2008. Tensilica Inc.

TIE: ユーザ定義I/O



- データパスをRTLとデータプレーンプロセッサの組み合わせで構成

© 2008. Tensilica Inc.

Design Support

- **Xplorer IDE**
  - Processor Configuration Development
  - Software Development
- **Automatic Generation of Processor Extension**
  - XPRES compiler
- **Automatic Generation of SW tools**
  - Processor Extensionに完全対応したツール生成
  - Compiler, Assembler, Linker, ISSISS
  - C/C++ API (XTMP), SystemC Model (XTSC)
- **EDA scripts generation**
  - Verification environment, Synthesis scripts

© 2008. Tensilica Inc.

ツールチェーンの自動化

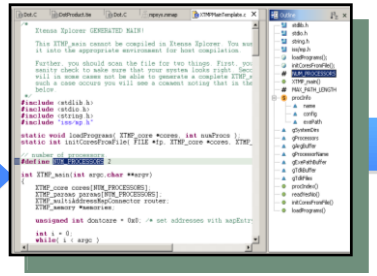
ANSI C/C++ Code

Source code

```
int main()
{
 int i;
 short c[100];
 for (i=0;i<N/2;i++)
 {
```

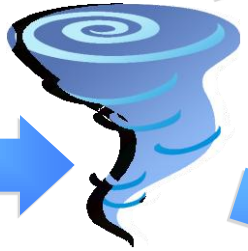
XPRES
Compiler

Optional Step



Processor Configuration

1. Select from menu
2. Explicit instruction description (TIE)
3. Automatic instruction discovery (XPRES)

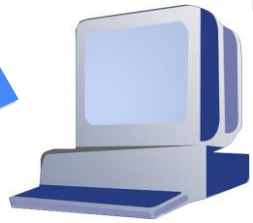


Xtensa
*Processor Generator **

Complete Hardware Design

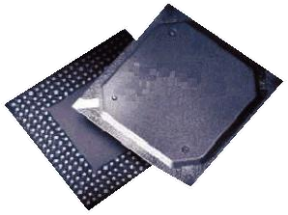
Source pre-verified RTL, EDA scripts, test suite

Processor Extensions



Customized Software Tools

C/C++ compiler
Debuggers,
Simulators
RTOSes



Use standard ASIC/COT design techniques and libraries for *any* IC fabrication process

Iterate in minutes!

You do not need to be a "processor expert". You only need to understand your target application.

** US Patent: 6,477,697*

© 2008. Tensilica Inc.

Tensilica Product Portfolio

	Controller	Comms DSP	HiFi Audio	Video/imaging	Other		
Fully customizable Cores	Xtensa controllers	Xtensa with Vectra DSPs	Xtensa with HiFi audio	Xtensa for Video	Data Comm	Storage	Security
Configurable Cores	Configurable Controllers	Configurable Vectra Comms DSP	Configurable HiFi Audio DSPs	Standard VDO 388VDO			
Standard Cores	Standard Controllers 106Micro, 108Mini, 212GP, 232L, 570T	Standard Comms DSPs 545CK	Standard Audio DSPs 330HiFi				

Processor Foundation

Core Xtensa Instruction Set and Base Processor

Xtensa Processor Generator (XPG) Automatic Processor Creation in 1 Hour

Complete Software Toolchain, 3rd Party Ecosystem, EDA Flows, Models

Multiple Processor SOC Design infrastructure

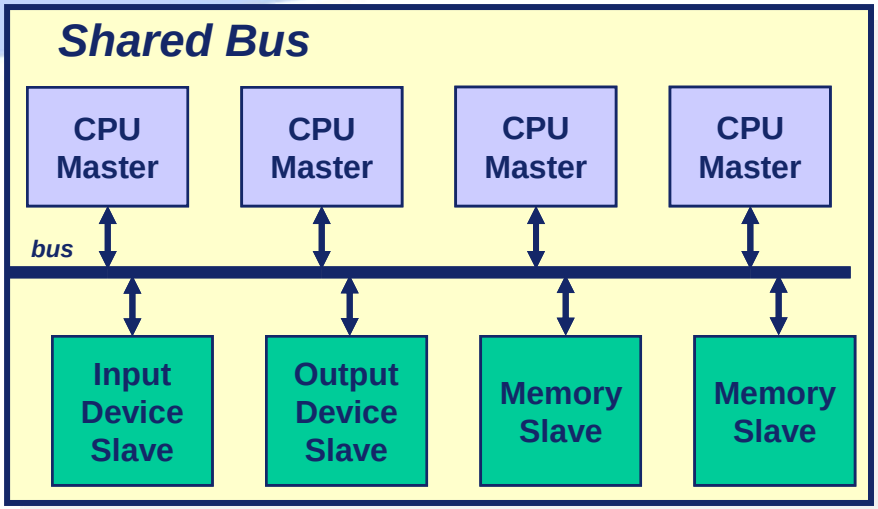
© 2008. Tensilica Inc.

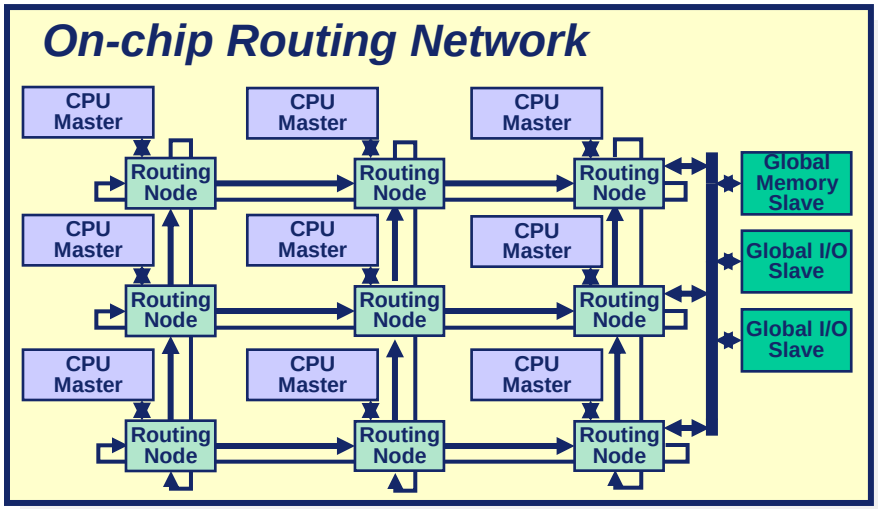
SoC platformとしての今後の課題

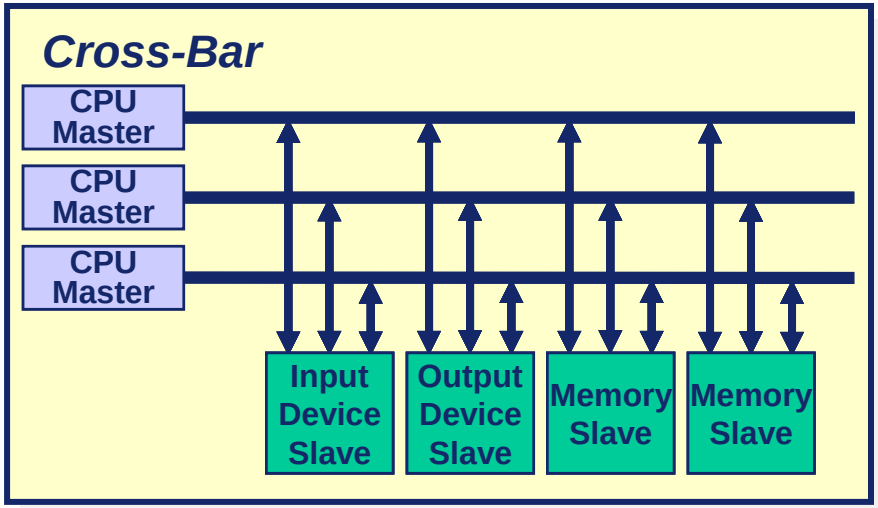
- **エコシステムの構築**
  - ソフトウェア資産の集積が課題
- **Extensibilityと汎用性のトレードオフ**
  - Extensibilityによる性能向上はSWの再利用性を妨げがち
- **マルチコアシステム構築の支援**
  - シングルコアとしてのcustomizable processor環境
  - マルチコアシステムは各アプリケーションに合わせて、アドホックに構築される
  - ソフトウェア開発環境が未対応

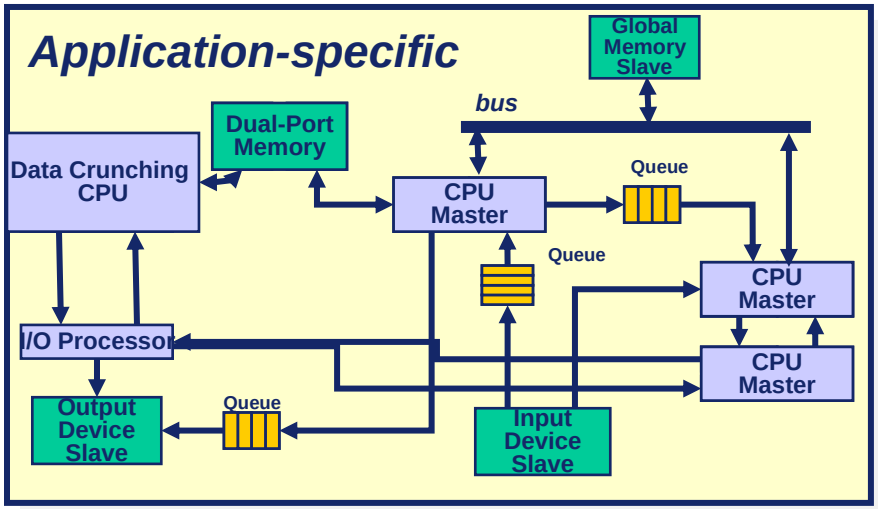
© 2008. Tensilica Inc.

様々なon-chip communications









© 2008. Tensilica Inc.

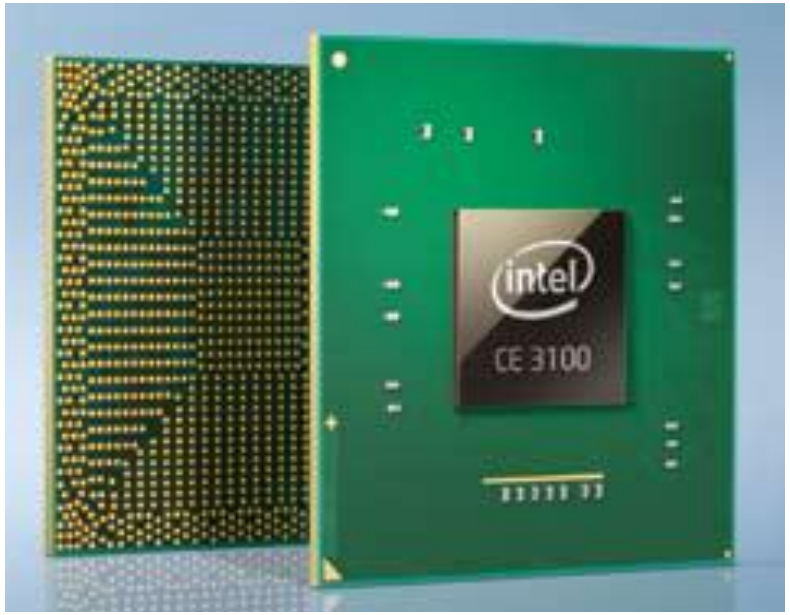
ユーザ適用事例

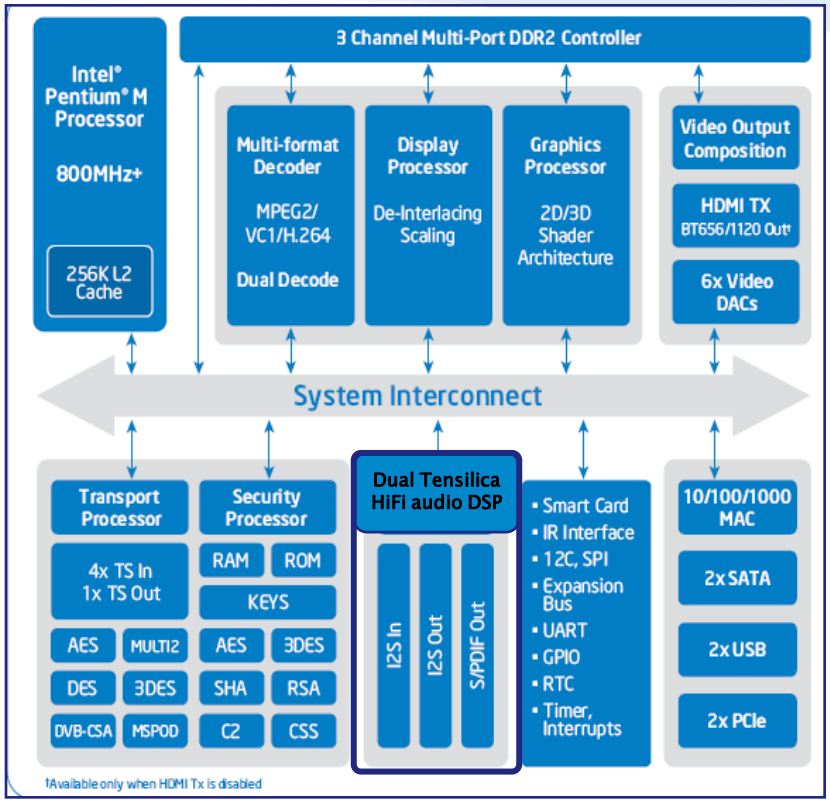
© 2008. Tensilica Inc.

Intel Adopts Tensilica HiFi2 Audio

Pentium M + Dual HiFi2 Audio DSP cores on 1 chip

Intel Media Processor CE3100





INTEL DEVELOPER FORUM August 20, 2008

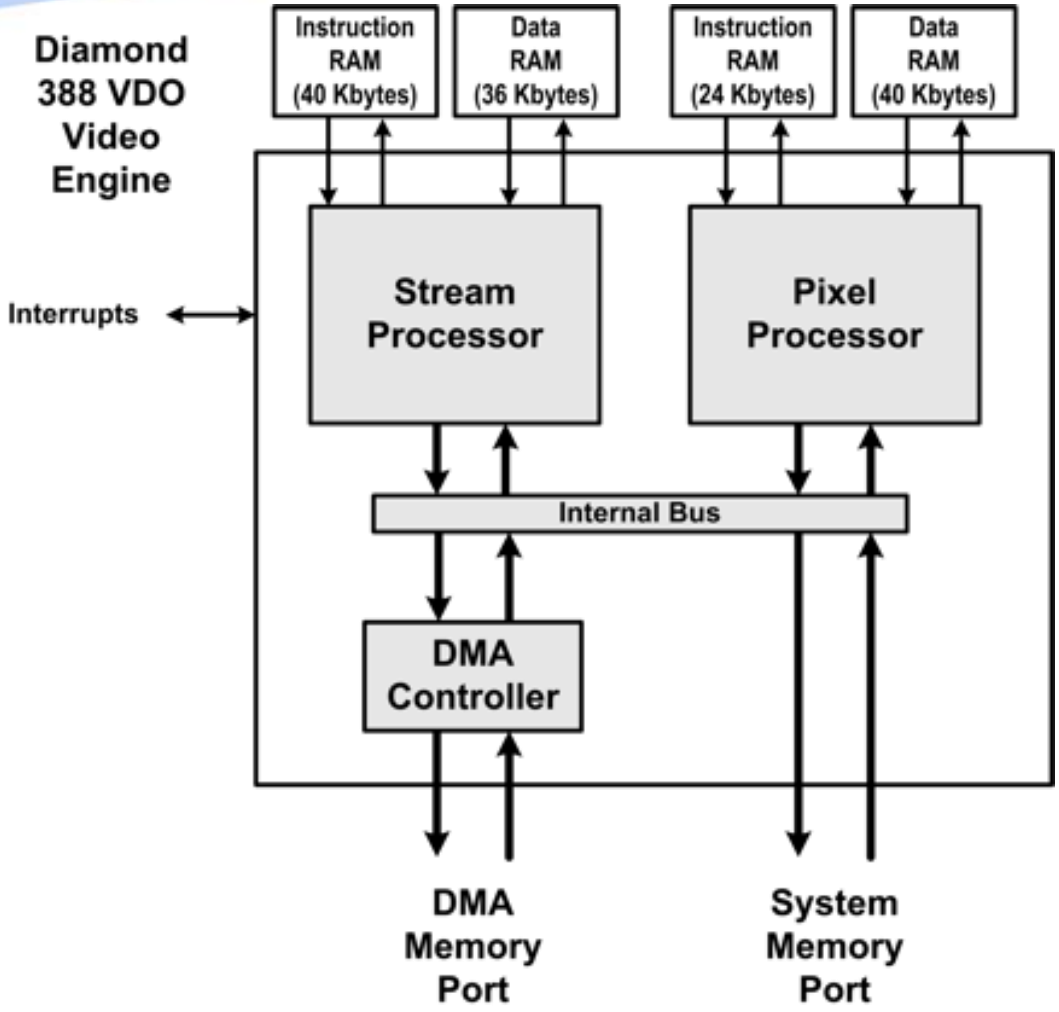
"At the Intel Developer Forum, Intel Corporation introduced the Intel® Media Processor CE 3100 [codename: Canmore], the first in a new family of purpose-built System on Chips (SoCs) for Consumer Electronics devices based on the company's popular Intel architecture (IA) blueprint […plus…] **multi-channel dual audio DSPs**."

"Dual 337 MHz Tensilica DSP cores with Tensilica Instruction Extensions (TIE), are used for advanced audio codecs with up to 7.1 channel output, supporting Blu-ray requirements independent of the [Pentium M] processor core."

Source: Intel Press release

© 2008. Tensilica Inc.

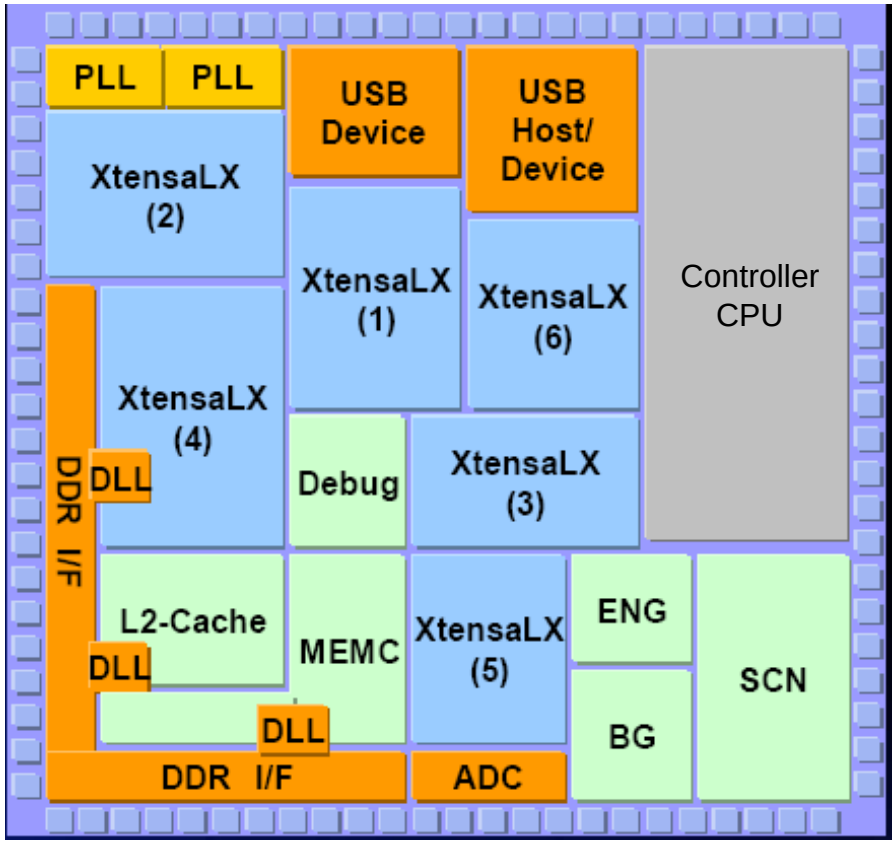
Tensilica
Diamond 388VDO Video Engine Core



© 2008. Tensilica Inc.

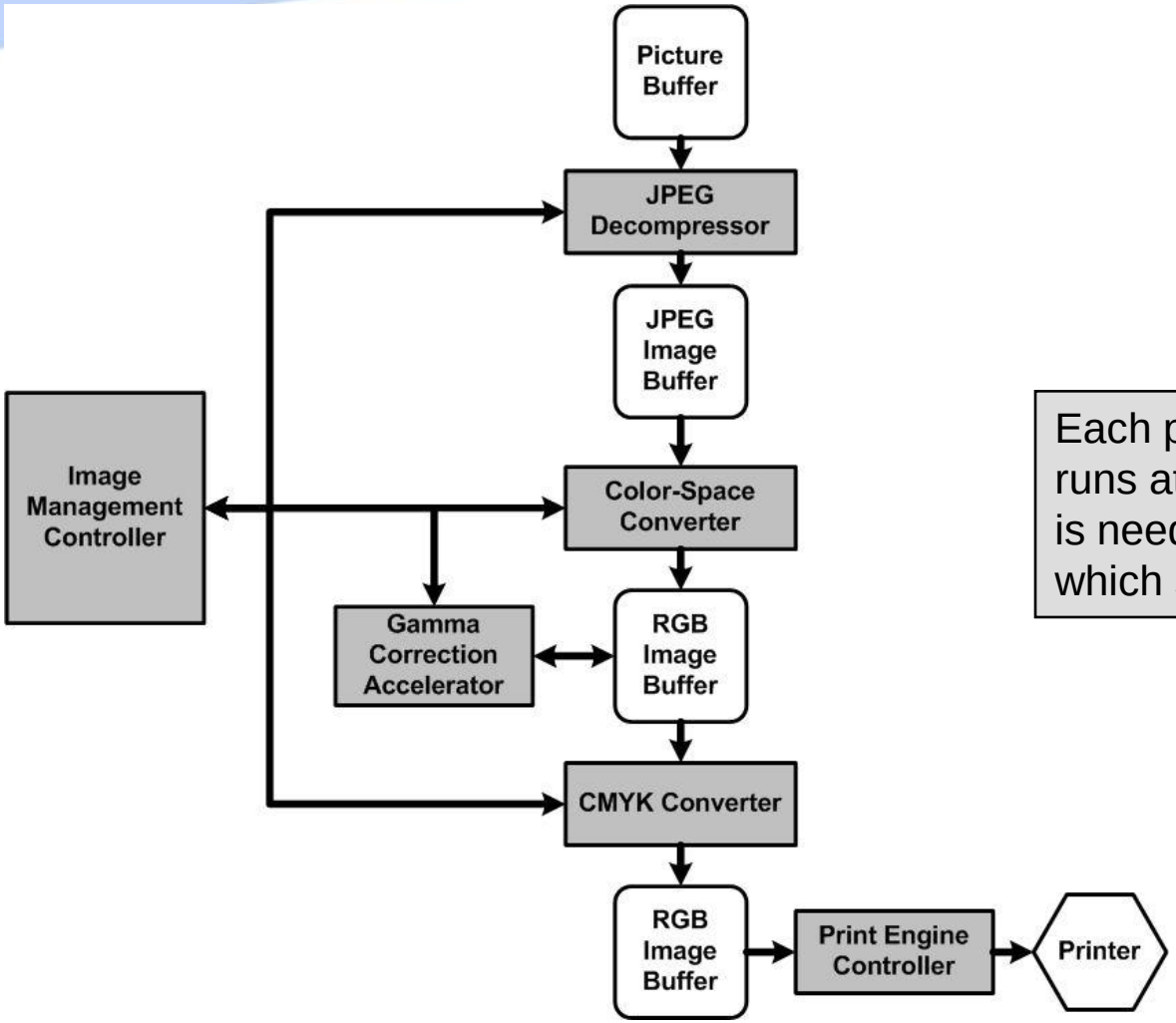
AMP example: Epson's REALOID Printer SOCs

- Heterogeneous, asymmetric, 7-CPU SOC design
- Very little RTL-designed HW
- 90nm process technology
- 288 MHz clock
- > 7M gates
- < 2.5W
- Used in Epson PM series printers



© 2008. Tensilica Inc.

AMP Printer Concept: SOC block diagram



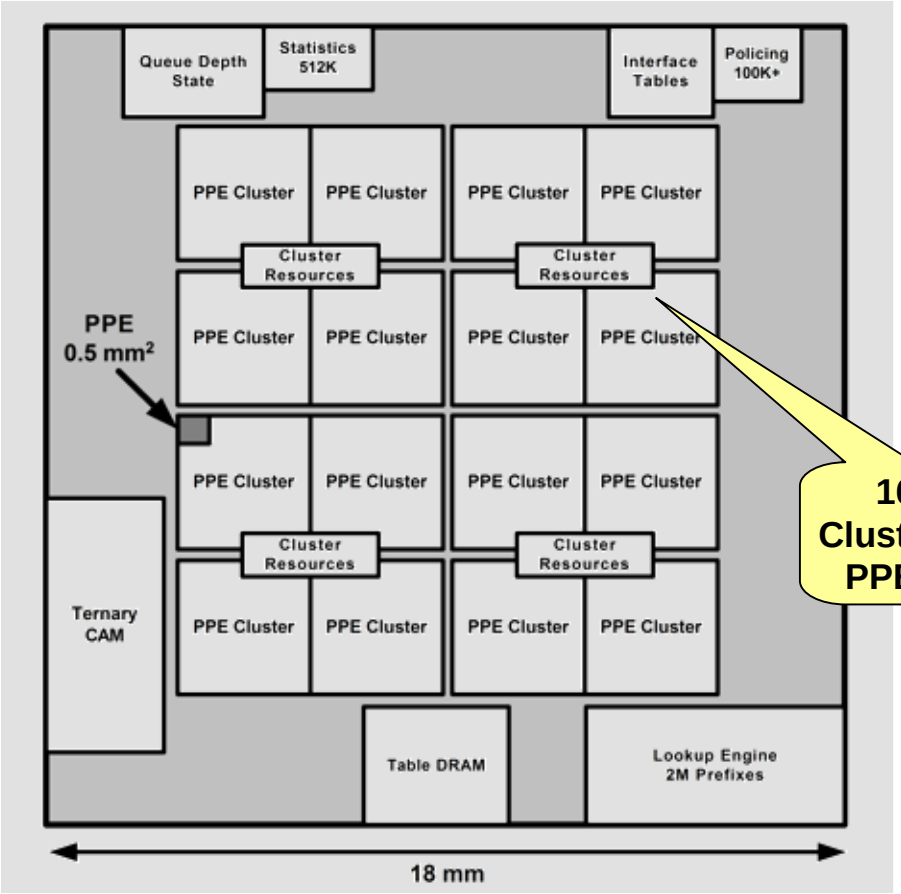
Each processing block runs at whatever clock rate is needed for that block, which saves energy.

© 2008. Tensilica Inc.

Embarrassingly Parallel Example:

Cisco's Silicon Packet Processor for IP Networking

- 192 Xtensa processor CPU cores
  - 4 CPUs for yield management (redundant processors)
- 18x18 mm chip
- 0.5 sq-mm per CPU core
- 18M gates
- 0.13 micron
- All data moves via intelligent DMA channels without a common bus
- Used in Cisco CRS-1 Carrier Routing System (Terabit router)



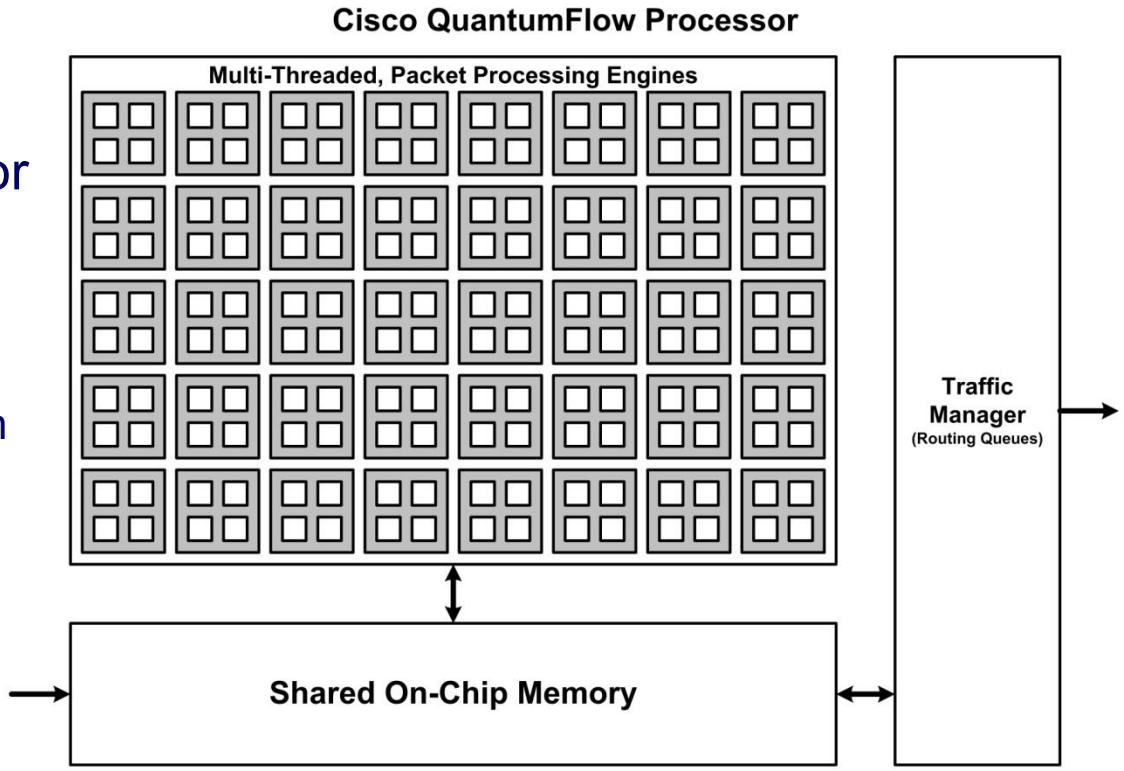
Massively parallel data (IP packets are not embarrassing!)

© 2008. Tensilica Inc.

Another Networking MP Example

Cisco's QuantumFlow Processor

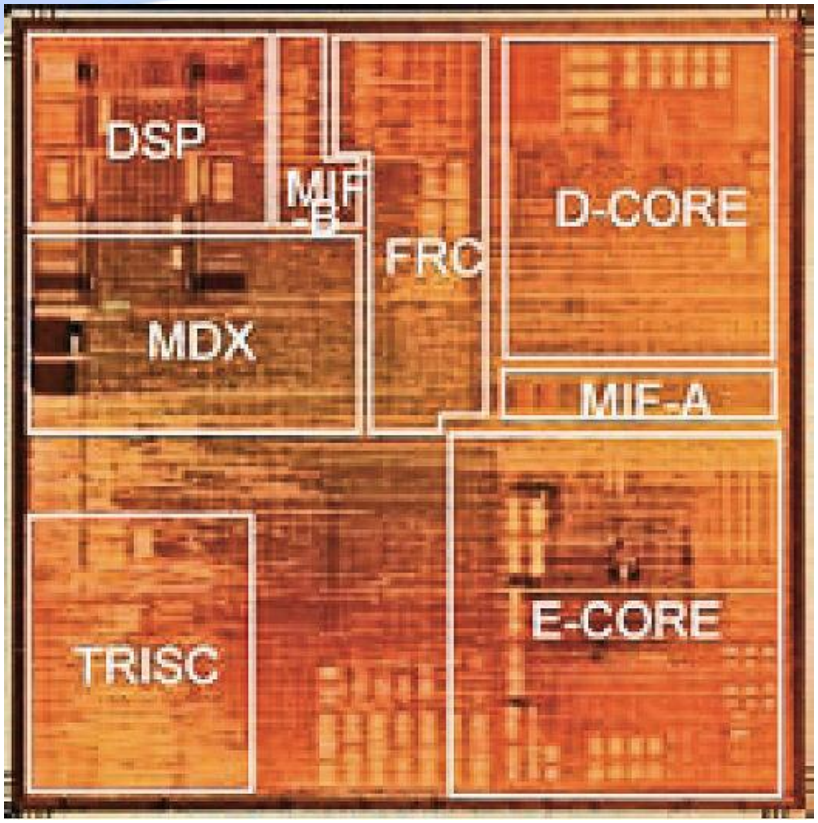
- 40 Xtensa processor CPU cores
- Each CPU is 4-way multithreaded
- 1.2 GHz clock
- Used in Cisco ASR 1000 Aggregation Services Router family



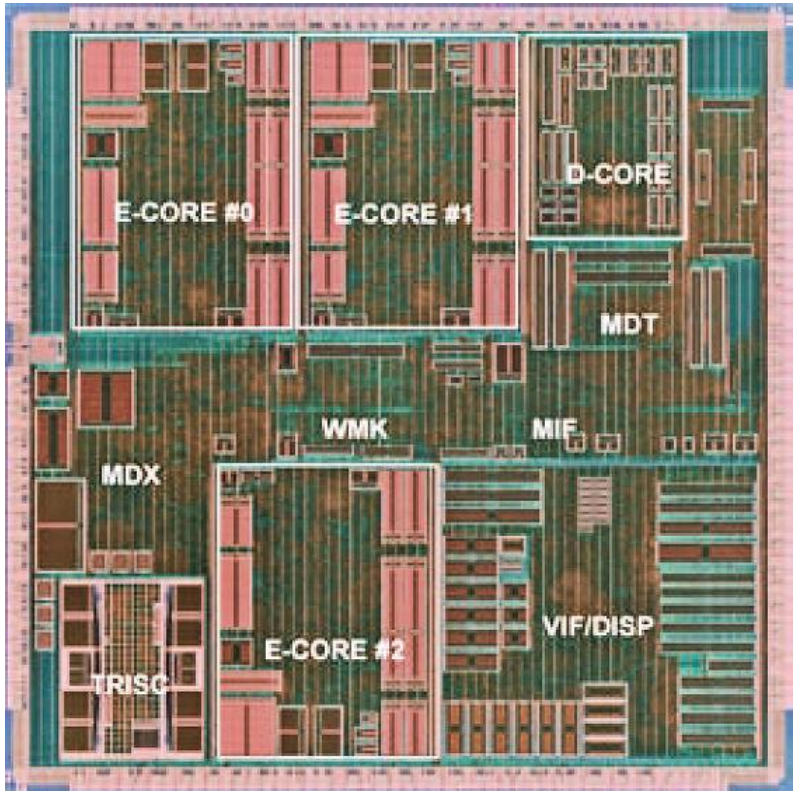
Massive data parallelism (IP packets are not embarrassing!)

© 2008. Tensilica Inc.

Multicore Video Chips



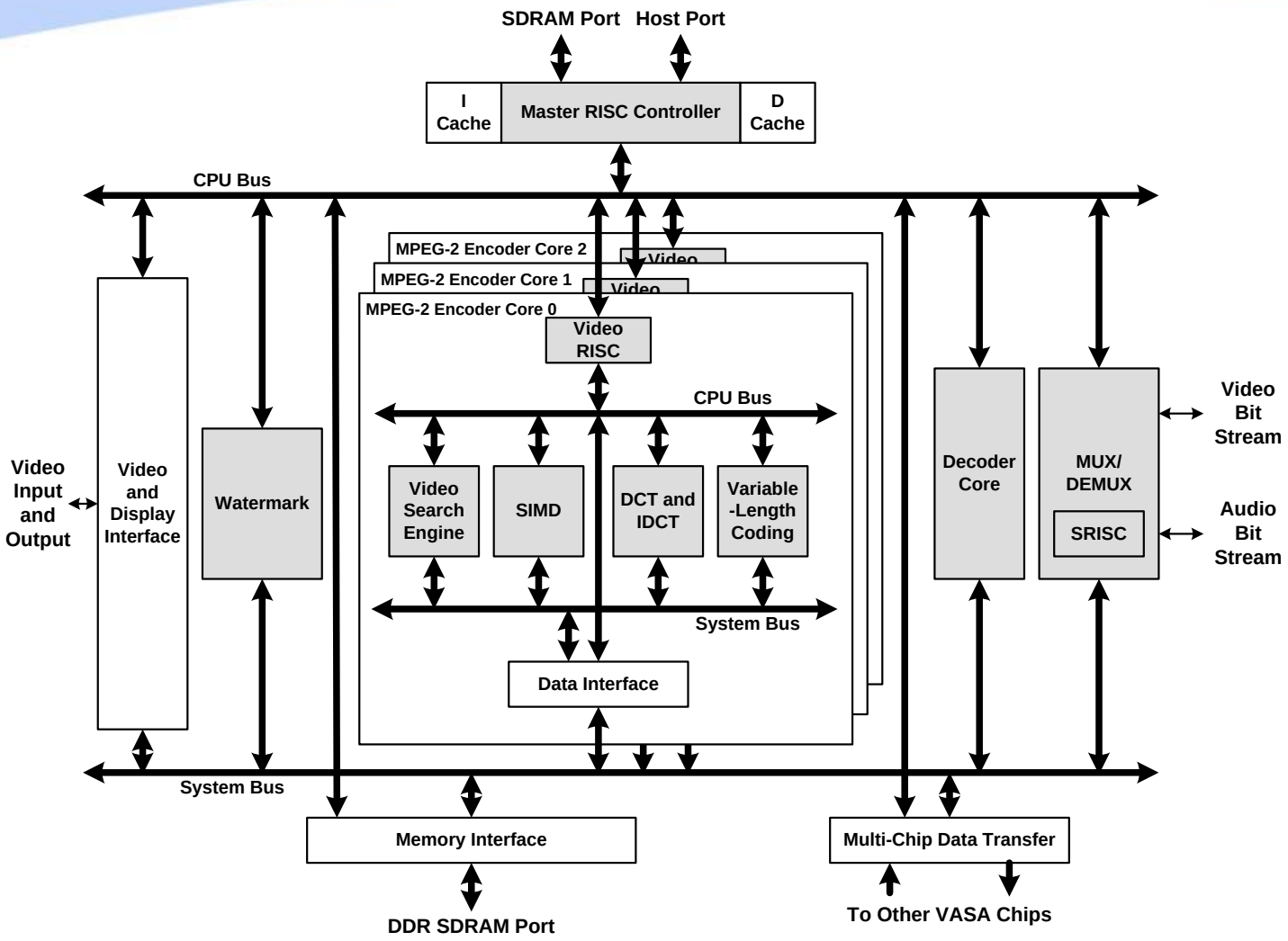
NTT SuperEnc III



NTT VASA

© 2008. Tensilica Inc.

NTT VASA Block Diagram



© 2008. Tensilica Inc.

まとめ

- **SOCプラットフォームへのcustomizable processorの適用**
  - 仕様変更、検証などのリスクを低減
  - アプリケーション向けにカスタマイズされたプロセッサは必要十分なパフォーマンスと低消費電力を実現
  - 特にDataplane(データインテンシブな処理)に向く
  - RTLと組み合わせてのデータパス構成が容易
- **マルチコアへの課題**
  - SOCは事実上マルチコア化
  - ソフトウェア開発環境の整備が必要

© 2008. Tensilica Inc.